AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1-8 (Cancelled)

9. (Withdrawn) A method for manufacturing a trench capacitor comprising:

forming a trench in a semiconductor substrate;

forming a first dielectric film on an inner surface of the trench;

filling a first doped amorphous silicon layer, doped with a first impurity, in the trench and having a first conductivity type;

removing the first doped amorphous silicon layer and the first dielectric film to a first depth to expose an inner wall of an upper portion of the trench;

forming a second dielectric film on the exposed inner wall of the trench;

selectively removing the second dielectric film from the bottom of the trench to expose a surface of the first doped amorphous silicon layer;

filling at least a second doped amorphous silicon layer, doped with a second impurity, in the trench, the second impurity, in the trench, the second impurity being different from the first impurity and having the first conductivity type;

etching back the second doped amorphous silicon layer to a second depth to remove an exposed second dielectric film; and

forming a buried strap layer on the second doped amorphous silicon layer, the buried strap layer being formed of the first doped amorphous silicon layer.

10. (Withdrawn) The method according to claim 9, wherein, a third doped amorphous silicon layer doped with the first impurity is filled in the trench before filling the second doped amorphous silicon layer.

11. (Withdrawn) The method according to claim 9, wherein the first impurity is arsenic and the second impurity is phosphorus.

12. (Withdrawn) The method according to claim 9, wherein the impurity concentration of the second doped amorphous silicon layer is varied.

13. (Withdrawn) The method according to claim 9, wherein the amount of the second doped polysilicon layer is varied.

14. (Withdrawn) The method according to claim 9, wherein after the second dielectric film is selectively removed from the bottom of the trench to expose the surface of the first doped amorphous silicon layer, the upper portion of the second dielectric film remaining on the inner wall of the upper portion of the trench is pre-treated to allow the second dielectric film to be thrusted back.

15. (Withdrawn) The method according to claim 14, wherein the second doped amorphous silicon layer is deposited on a reduced thickness portion of the second dielectric film.

16. (Withdrawn) The method according to claim 14, wherein a part of the buried strap layer is positioned at the reduced thickness portion of the second dielectric film.

17. (New) A trench capacitor comprising:

a semiconductor substrate;

a trench formed in the semiconductor substrate;

a first doped polysilicon layer filled in the trench through a first dielectric film and doped with a first impurity having a first conductivity type;

a second doped polysilicon layer filled in the trench through a second dielectric film, formed on the first doped polysilicon layer and doped with the first impurity having the first conductivity type;

a third doped polysilicon layer formed on the second doped polysilicon layer through the second dielectric film and doped with a second impurity having the first conductivity type, the second impurity being different from the first impurity and having a greater diffusion coefficient than that of the first impurity; and

a fourth doped polysilicon layer provided in the trench, formed on the third doped polysilicon layer and doped with the first impurity having the first conductivity type.

18. (New) The trench capacitor according to claim 17, wherein the first impurity is arsenic and the second impurity is phosphorus.

19. (New) The trench capacitor according to claim 17, wherein the fourth doped polysilicon layer is a buried strap layer.

20. (New) The trench capacitor according to claim 17, wherein the impurity concentration of the second doped polysilicon layer is varied.

21. (New) The trench capacitor according to claim 17, wherein the amount of the second doped polysilicon is varied.

22. (New) The trench capacitor according to claim 17, wherein the first dielectric film is a silicon nitride film.

23. (New) The trench capacitor according to claim 17, wherein the second dielectric film is a collar oxide film.

24. (New) The trench capacitor according to claim 17, wherein a buried strap junction edge is covered with phosphorus.